



5. 中英文摘要

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L	imate and cost. The radius of the radius	D			
1 1 2 1 3 1 4	cavities; a value of 1 in a particular location means that cavities are completely filled in that region. We have achieved completely filled cavities, i.e., value of 1 at all locations. We have achieved RLT around 10mm and even RLT at all location in pattern using rm-17020E photoresist imprint. GaN GAA Nanowire: To increase typically low output drive currents from Si Nanowire field-effect transistors (FETs), we show a GaN based GAA Nanowire FET's effectiveness. The theoretical study is focused on the three dimensional device designs, comparisons, random dopant fluctuation using IFM, and general variability issues including nanowire length, gate work function, and channel thickness are discussed. Performance of GaN GAA Nanowire is found to be increasing as Gate length is increased. Electrical characteristics of FETs including threshold voltage saturation, On/Off current ratio and sub threshold slope (SS) are analysed. GaN GAA structure let to gate control ability improvement compared to Si based Nanowire in electrical performance.			E	
1 3 1 8 1 7 1 6 1 5 1 4 1 3 1 2 1 1 1	Nanoimprint Lithography: Si master molds are generally patterned by electron-beam lithography (EBL) that is known to be a time consuming nano patterning technique. Thus, developing mold duplication process based on high throughput technique such as nanoimprint lithography can be helpful in reducing its fabrication time and cost. This study aims to develop capabilities in patterning nano structure using thermal nano-imprint lithography. The NEB22 A2, m- I7000E series negative e-beam resist possess a variety of characteristics desirable for NL, such as low viscosity, low bulk-volumetric shrinkage, high Young's modulus, high thermal stability, and excellent dry-etch resistance. The excellent oxygen-etch resistance of the barier material enables a final transfer pattern that is about three times higher than that of the original NIL mold. Based on these imprint on negative photo resist approach is used for pattern transfer into silicon substrates. The result is a high-resolution pattern with feature sizes in the range of nanometer to several microns. We combine Simprint Core simulation software for simulation nanoimprint process and to achieve uniform RLT. Our research results in low RLT as 10-20nm thicknesses for mr-17020E photoresist. The simulation results and experimental results are matching. A plot of how RLT across the whole stamp region changes with imprinting duration is shown using simulation. The central, thick line shows the average RLT across the entire stamp; the thin lines indicate the stamp-average RLT plus and minus one standard deviation of the cross-stamp RLT values. Simulated and calibrated for uniform residual layer thickness (RLT) and the cross-sections of RLT are plotted. In cavity filling value of 0 denotes completely empty cavities; a value of 1 an a particular location means that cavites are completely filled in that region. We have achieved completely field cavities, i.e., value of 1 at al locations. We have achieved RLT around 10mm and even RLT at all location in pattern using mr-170020E				=

6. 確認貼上目錄/圖目錄/表目錄

基本資料 中外文摘要 目錄 参考文獻 電子全文 備份全文



7. 參考文獻查核

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